A New EEPROM Architecture for High-Density Application

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Introduction

Electrically erasable and programmable read-only memory (EEPROM) has become very common over the last decade. Decreasing the size of memory is one major key of the new technology evolution. In typical FLOTOX EEPROM, each cell is composed of a select transistor in series with the memory transistor. This limits the shrinkage of EEPROM dimensions and the lifetime of the cell [1].

Moreover, during writing operation a high positive signal is applied on the drain, source is floating while control gate and substrate are grounded. The junction drain-substrate is reverse biased and a leakage current due to band-to-band tunneling is detected between drain and substrate increasing the cell consumption. In the same time hot hole injection can degrade cell reliability [2] [3]. In this paper we propose a new cell without select transistor with new working conditions.

Concept of the cell

This concept is based on two different injection ways during erasing and writing operation in order to increase reliability of the cell. Moreover, the new cell layout must cancel the band-to-band tunneling during write operation [4]. Layout of top of view and cross-section views of the cell are shown in fig. 1. The first layer of polysilicon is used to form a floating gate memory transistor. A second layer of polysilicon forms the two control gates: a short gate that has a weak coupling effect and a large gate that has a strong capacitive coupling to the floating gate. The two layers of polysilicon are separated by a 15nm ONO inter-poly isolation, and the first oxide level is a thin tunnel oxide (<10nm). Finally, the two control gates are isolated by oxide. Figure 2 shows the electrical equivalent circuit of the cell without mechanism of electron tunneling, where C_{PP1} (resp. C_{PP2}) is the inter-poly capacitor between floating gate and large gate (resp. short gate), C_D the floating gate overlap capacitor on the drain. C_{ox} is the MOS capacitor.

Cell operation

This new cell is erased, like standard EEPROM cell, by applying a positive high signal (V_{pp}) on both control gates, drain, source and substrate are grounded. The writing operation is performed by applying a negative signal (V_{CV}) to the large gate, P-well and bit line to pull down the floating potential. In the same time, we apply a large positive signal on the short gate to generate tunnelling current through ONO, from floating gate to the short control gate. In read mode, p-well, source line and short control gate are grounded. The large control gate is biased to ~5V (V_{DD}) and the bit line is biased to create a drain-source potential difference of ~1V. These operations are summarized in Figure 3.

Cell modeling

The approach used to develop the model is based on the charge sheet approximation [5] [6]. This model is a compact floating gate memory model which can be used to analyse cell electrical behaviour. With this model, we can simulate both transient and static characteristics. MOSFET description based on Pao and Sah allows the physical parameters continuity between all regimes and the channel spatial resolution of electrical field and inversion charge. The figure 4 shows an erase/write operation in which we can observe the variation of the threshold voltage V_T and signals applied on the large gate (V_{CGL}) and short gate (V_{CGS}). During the erase operation, the threshold voltage increase to 4 V due to the charge injection into the floating gate. In case of write operation V_T decreases to –0.6 V due to the tunneling current between floating gate and short control gate. Simulated programming window (4.6V) prove a good behavior of this new cell in simulation.

Electrical characterization

Fig. 5.a and 5.b show $I_{DS}(V_{CGL})$ characteristics with variation of the short gate potential (V_{GCS} = -3V to 3V). These characteristics are shifted under short gate coupling effects. With these curves, parameters of compact model have been extracted to calibrate coupling ratio of each control gates and we obtain a good correlation between measure and simulation. Figure 6 presents measurements at V_{DS} = 0.1V of the programming window. The magnitude of this window is approximately 4.5V and confirms the good fonctionnality of this memory point.

Conclusion

In conclusion, we have proposed a new device architecture which allows a cell programmation by the top of the structure. This concept induces the elimination of the select transistor. Simulation results confirm that the general concept of the novel EEPROM cell is operational and a compact model proposed can be exploited in order to improve the cell behavior. A first prototype has been realized, and preliminary electrical results are in good correlation with simulations, other electrical test must be realized like endurance and retention test. Scalability and endurance potentiality make this cell interesting for future high-density and high reliability applications.

References

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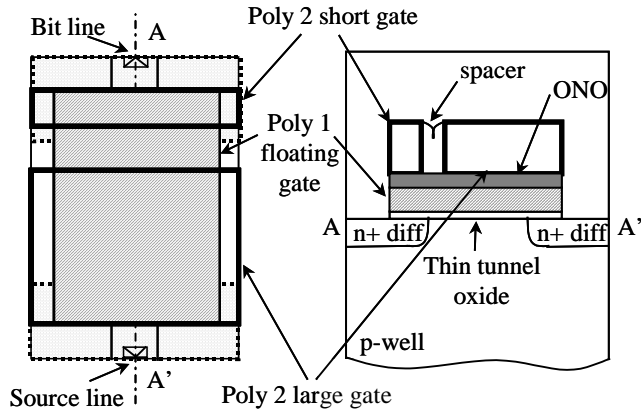[6] R. Bouchakour et al., JNCS, 280, p.122-126, 2001 Mc Graw Hill Int. Edition, 1999
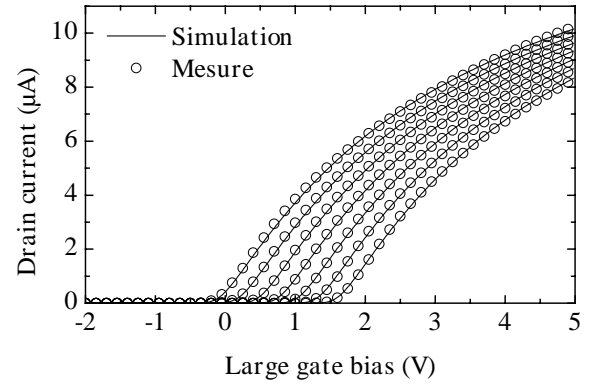
Figure 1: Top and cross-section drawings of the cell

Figure 2: Electrical equivalent circuit of the cell

Figure 3: a. Erase operation b. Write operation

Figure 4: Transient simulations of write/erase operations

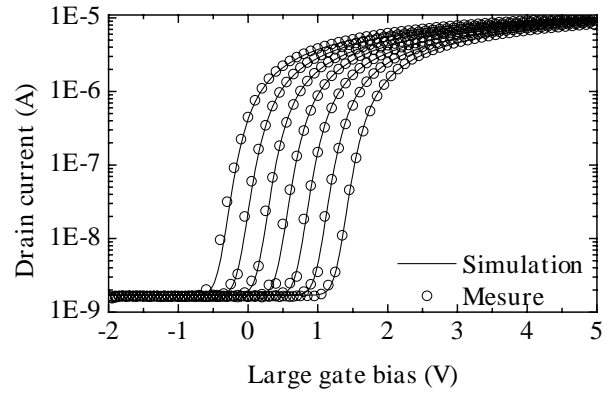Figure 5.a: Short gate bias (V_{GCS} = -3V to 3V) influence on $I_{DS}(V_{CGL})$ characteristics

Figure 5.b: Short gate bias (V_{GCS} = -3V to 3V) influence on $I_{DS}(V_{CGL})$ characteristics with logarithmic scale
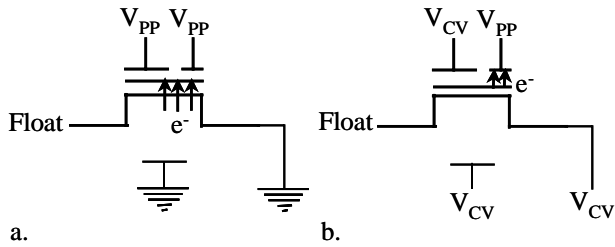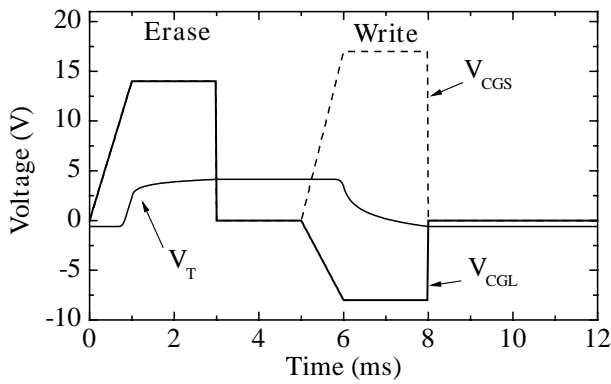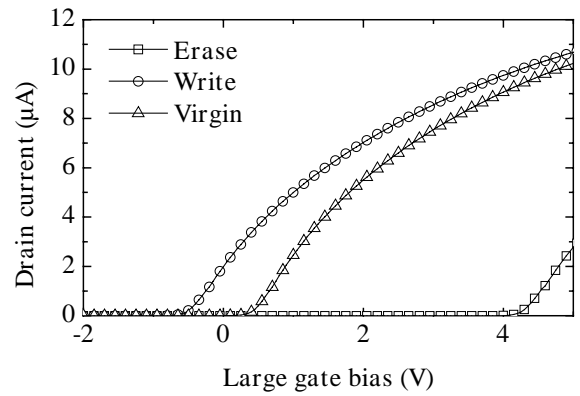

Figure 6: Programming window measurement of the cell at V_{DS} = 0.1V